

REMARKS/ARGUMENTS

Claims 1-21 and 25-31 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the following combination of references: over *Giboney et al.* (U.S. Patent No. 6,318,909) (hereinafter *Giboney*), *Ohno et al.* (U.S. Patent No. 6,923,580) (hereinafter *Ohno*); *Lee et al.* (U.S. Patent No. 6,821,027) (hereinafter *Lee*); *Hargis et al.* (U.S. Patent No. 6,792,171) (hereinafter *Hargis*); and *Nguyen et al.* (U.S. Patent No. 6,707,140) (hereinafter *Nguyen*).

Claims 1-6 are amended herein. Claims 22-24 and 29-31 are cancelled without prejudice. Claims 32-37 have been added to capture certain patentable subject matter. Accordingly, based on the above amendments and the following remarks, the applicants respectfully request reconsideration of this application.

General considerations

As pointed out in prior actions, the claims recite a pair of generally parallel circuit boards that include one board configured as an optical port and another as an electrical port. The boards are arranged to include an offset between the optical port and the electrical port to enable a wide range of adaptability to various formats and form factors while using similar components.

Thus, the arrangement includes a first board with an optical port facing in one direction with the electrical connections facing in an opposite direction. These electrical connections are connected to a second electrical interface board that has pluggable electrical features on its backend. The second board's height can be adjusted as needed (enabling the same basic components to be quickly and easily adapted to a wide range of varying formats and form factors) due to the flexible electrical connector between the boards. Additionally, a support block can be used to orient and connect the photonic devices with the chip package. Certain particular details are unique and present new approaches not found in the cited references. This is especially the case in the amended claims. Accordingly, it is respectfully submitted that these claims as amended should be allowable.

Rejections Under 35 U.S.C. § 103

Claims 1, 8, 13-21, 29, & 31:

Claims 1, 8, 13-21, 29, & 31 stand rejected under 35 U. S. C. § 103 as being unpatentable over *Giboney* in view of *Ohno*. Several claims have been amended to address these claim rejections.

Claims 29 and 31 have been cancelled, thus, as to those claims this ground of rejection has been made moot. Accordingly, applicants respectfully request that this ground of rejection be withdrawn.

The applicants point out that the cited rejection offers *Giboney* (20:2-6) as teaching “a first rigid substrate having electrical traces”. The actual language of Claim 1 is significantly different from that narrow description, the actual language is “a planar first substrate having a top surface and a bottom surface, electrical traces, a port end, and an interior end”. Quite frankly, the cited portion of *Giboney* does not refer to any figures “(not shown)” and does not describe “electrical traces, a port end, and an interior end”. Since the particular arrangement of components in this invention is rather important, this shortcoming of the cited reference can not be said to teach or suggest the claimed first substrate. Such a shortcoming is fatal to a *prima facie* case of obviousness.

At the very most it could be said that *Giboney* teaches a “support block having a first face and a second face”. And even this reading may be over stepping what *Giboney* actually describes.

However, Claim 1 has been substantially amended to clearly highlight several structural distinctions between the claimed invention and the cited references. *Giboney* states that “a printed circuit board assembly (not shown) can be attached by suitable conductors to connections available on the exposed areas of the portion 92. *Giboney* (20:2-6). Upon review of *Giboney* (Fig. 9) it is clear that this “substrate” must be mounted on top of the “support block”. This is exactly the opposite of the configuration recited in Claim 1 which recites “an opto-electronic device attached to and electrically connected to the top surface of the first substrate”.

In another example, Claim 1 has been amended to recite “a semiconductor chip package having a top surface and a bottom surface with top and bottom electrical contacts, the bottom

surface mounted ... directly on the top surface of the first substrate with the bottom electrical contacts at the bottom surface of the chip package being electrically connected to the electrical traces of the first substrate". This configuration describes a functional configuration not taught or suggested by *Giboney* where the chips 92 are described as being on top of the "support block" 29. This particular configuration becomes even more troublesome when one seeks to combine this reference with *Ohno* (as will be described in more detail below). And of course as readily admitted in the Action, the *Giboney* reference fails entirely to address the issue of a second backend electrical connector substrate and a flex electrical connector.

Ohno is offered to correct these shortcomings of *Giboney*. For example, the Action states that *Ohno* teaches "a second substrate having electrical traces, the second substrate having a port end and an interior end, wherein the port end forms the electrical port" and "a flex connector ... containing a plurality of electrically conductive ... whereby the flex connector allows for the adjustable positioning of the height of the optical port with respect to the height of the electrical port". Firstly, there is no teaching or suggestion of height differential adaptability in *Ohno*. Thus, *Ohno* misses a critical point of the invention. Additionally, the applicants note that the first substrate 101 of *Ohno* does not teach "a semiconductor chip package ... mounted ... directly on the top surface of the first substrate" nor "a support block for supporting an optical device package, the support block having a first face and a second face that are angled relative to one another ... wherein the first face of the support block is mounted on the top surface of the chip package". This is important because critical features of *Ohno* are the heat radiating fins 601 and the heat conductors 611, 612, 613 which sink heat from the boards and components (201, 202, 203, 204, 101, 102, 103 and so on). See, throughout the *Ohno* Specification and Claims 1-20. This heat sink and conductors that contact almost all of the "substrate" surface would prevent the attachment of the claimed "semiconductor chip package ... mounted ... directly on the top surface of the first substrate" and also prevent the mounting of the "support block ... on the top surface of the chip package". Thus, at best the combination of *Ohno* and *Giboney* teach a non-operative invention. More likely still is the fact that such a grave limitation *Ohno* teaches away from a combination with *Giboney*.

Thus, as to Claim 1, the applicants respectfully submit that the cited portions of *Ohno* and *Giboney* fail to teach or suggest all the recited limitations (e.g., top mounted die and support block and so on) and so therefore fail to establish a *prima facie* case of obviousness. Moreover,

even if a reasonable argument could be made that all claim limitations are taught in the cited art, there is no motivation to combine the references due to non-operability and teaching away.

Accordingly, the applicants request that withdrawal of this ground of rejection as to Claim 1. Moreover, for at least the forgoing reasons, the dependent claims are also believed allowable. Many more separate arguments in favor of patentability could be advanced in favor of the dependent claims. But, due to the underlying sufficiency of the arguments supporting Claim 1, these arguments are not deemed necessary at this time. Accordingly, the applicants request that this ground of rejection be withdrawn as to dependent claims 8 & 13-21 (and also cancelled Claims 29 and 31).

Claims 2 and 3:

Claims 2 and 3 have been rejected under 35 U. S. C. § 103(a) as being unpatentable over *Giboney* and *Ohno*, in view of *Hargis et al* (USPN 6,792,171 hereinafter "*Hargis*"). As explained above with respect to Claim 1 (upon which Claims 2 and 3 depend) *Giboney* and *Ohno* are deficient references that do not teach all the claim limitations as required under §103. For example, *Giboney* and *Ohno* do not teach a "a semiconductor chip package ... mounted ... directly on the top surface of the first substrate" nor "a support block for supporting an optical device package ... wherein the first face of the support block is mounted on the top surface of the chip package". Absent these, and other, limitations the *Giboney* and *Ohno* combination of references fails to establish a *prima facie* case of obviousness as to the rejected claims. Nothing in *Hargis* rectifies these shortcomings. Moreover, the applicants respectfully submit that no suggestion has been provided that would lead one of ordinary skill to combine the references in the manner suggested in the rejection. Consequently, no reasonable combination of the *Giboney*, *Ohno*, and *Hargis* references provides grounds for rejecting the pending claims. Accordingly, the applicants request that the pending claim rejections concerning claims 2 and 3 be withdrawn.

Claims 4-6 and 8-11:

Claims 4-6 and 8-11 have been rejected under 35 U. S. C. § 103(a) as being unpatentable over *Giboney* and *Ohno*, in view of *Nguyen*. As explained above with respect to Claim 1 (upon which Claims 4-6 and 8-11 depend) *Giboney* and *Ohno* do not teach all the claim limitations as required under §103. For example, *Giboney* and *Ohno* do not teach a "a semiconductor chip package ... mounted ... directly on the top surface of the first substrate" or "a support block for

supporting an optical device package ... wherein the first face of the support block is mounted on the top surface of the chip package". Absent these, as well as other, limitations the *Giboney* and *Ohno* references fail to establish a *prima facie* case of obviousness as to the rejected claims. Nothing in *Nguyen* rectifies these shortcomings. Consequently, no reasonable combination of the *Giboney*, *Ohno* and *Nguyen* references provides grounds for rejecting the pending claims. Accordingly, the applicants request that the rejection of claims 4-6 and 8-11 be withdrawn.

Claims 7, 28, and 30:

Claims 7, 28, and 30 have been rejected under 35 U. S. C. § 103(a) as being unpatentable over *Giboney*, *Ohno*, and *Nguyen*, in view of *Hargis*.

Claim 30 is cancelled, thus, as to those claims this ground of rejection has been made moot. Accordingly, applicants respectfully request that this ground of rejection be withdrawn as to Claim 30.

As explained above with respect to Claim 1 (upon which Claim 7 depends) *Giboney* and *Ohno* do not teach all the claim limitations as required under §103. For example,

Giboney and *Ohno* do not teach a "a semiconductor chip package ... mounted ... directly on the top surface of the first substrate" or "a support block for supporting an optical device package ... wherein the first face of the support block is mounted on the top surface of the chip package". Absent these, and other, limitations the *Giboney* and *Ohno* references fails to establish a *prima facie* case of obviousness as to the rejected claims. Nothing in *Hargis* or *Nguyen* rectifies these shortcomings.

However, the applicants point out the inventive Specification has pointed out the value of the close spatial proximity of the converter to the optical devices whose signals are being converted. Thus, such proximity is valuable, as claimed in Claim 7, "an electrical converter that is located on the second face of the support block such that single ended signals travel between the photonic device and the electrical converter". This both the photonic device and the converter are located close to on another on the same support block.

The statement in the Action that such a modification "would have been obvious" is impermissible absent a suggestion of such a limitation in the cited art.

Putting aside the fact that the references do not teach or suggest the claimed invention, this grounds for rejection is specifically deficient because it has failed to provide a valid motivation to combine the references. The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). If, as in this case, the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the examiner to explain why the combination of the teachings is proper. *Ex parte Skinner*, 2 USPQ2d 1788 (Bd. Pat. App. & Inter. 1986). In the present case, the Office Action has not satisfactorily explained why the suggested combination is proper.

The Office Action, as its sole rationale for combining the references, states "[i]t would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the electrical converter for transmitting signal as taught by Hargis". This line of reasoning is expressly forbidden by the case law. "The level of skill in the art cannot be relied upon to provide the suggestion to combine references." *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999)(emphasis added). "A statement that modifications of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)(emphasis original). There is no suggestion in any of the cited references indicating that they should be combined. Additionally, the motivation to combine is provided by the teachings of the applicants' Specification. This is also an impermissible hindsight application of the teachings of the invention.

In view of the foregoing, the cited references fail to establish a *prima facie* case of obviousness as to Claim 7. Moreover, for at least the same reasons, the cited references fail to establish a *prima facie* case of obviousness as to Claim 28.

Accordingly, there is no teaching of this limitation and no motivation to combine the references as “suggested” in the Action. Absent these limitations, the cited combination of references fails to establish a *prima facie* case of obviousness as to the rejected claims. Consequently, no reasonable combination of the *Giboney*, *Ohno*, *Nguyen*, and *Hargis* references provides grounds for rejecting the pending claim 7. Accordingly, the applicants request that the pending claim rejections concerning claims 7 and 28 be withdrawn.

Claims 25 and 27:

Claims 25 and 27 have been rejected under 35 U. S. C. § 103(a) as being unpatentable over *Lee*, in view of *Giboney*. With respect to Claim 25, the applicants respectfully submit that the cited portions of the references do not teach or suggest “an intermediate substrate containing a plurality of electrically conductive traces, wherein the intermediate substrate connects the electrical traces within the first and the second substrates, wherein a thickness of the intermediate substrate separates the height of the optical port with respect to the height of the electrical port by a desired distance” (emphasis added). *Lee* is restricted to an elastomeric conductor not “an intermediate substrate containing a plurality of electrically conductive traces”. Such an elastomeric material would not and could not define a stable separation distance between the two substrates.

Additionally, Claim 25 is rejected by *Lee* alone and *Lee* alone does not teach an “optical device package mounted on the second face of the support block, the optical device package having at least one active facet thereon and having electrical contacts that are electrically coupled to associated traces on the support block”. Thus *Lee* alone cannot support a *prima facie* case of obviousness as to Claim 25. Also, Accordingly, *Lee* does not teach or suggest Claim 25.

As to Claim 27, the combination of *Lee*, in view of *Giboney* do not teach all the claim limitations as required under §103. For example, *Giboney* and *Lee* do not teach “an intermediate substrate containing a plurality of electrically conductive traces, wherein the intermediate substrate connects the electrical traces within the first and the second substrates, wherein a thickness of the intermediate substrate separates the height of the optical port with respect to the height of the electrical port by a desired distance”.

Accordingly, absent these, and other, limitations the *Giboney* and *Lee* references fail to establish a *prima facie* case of obviousness as to the rejected claims. Consequently, no reasonable combination of the *Giboney* and *Lee* references provides grounds for rejecting the

pending claims. Accordingly, the applicants request that the pending claim rejections concerning claims 25 and 27 be withdrawn.

Claim 26:

Claim 26 has been rejected under 35 U. S. C. § 103(a) as being unpatentable over *Lee*, in view of *Giboney* and *Hargis*. As explained above with respect to amended Claim 25 (upon which Claim 26 depends) neither *Giboney* nor *Lee* does not teach all the claim limitations as required under §103. Nothing in *Hargis* remedies these shortcomings. Accordingly, the applicants request that withdrawal of this ground of rejection as to Claim 26.